Digital Design Diploma

# **Assignment 2**

# **Combinational & Sequential Logic Design**

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| **Group** | G2 |

**Submitted to: Eng. Kareem Waseem**

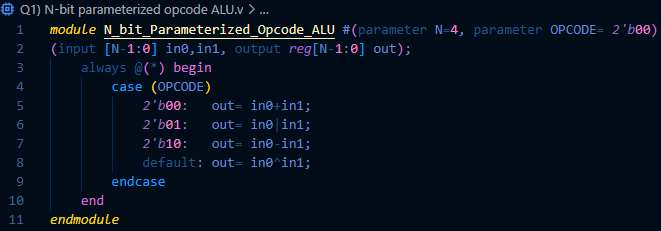
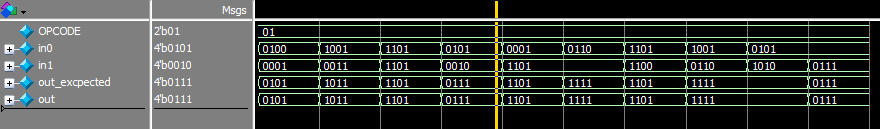
1. **N-bit Parameterized Opcode ALU:**

Figure 2: Q1 Wave (Addition)

Figure 1: Q1 Code

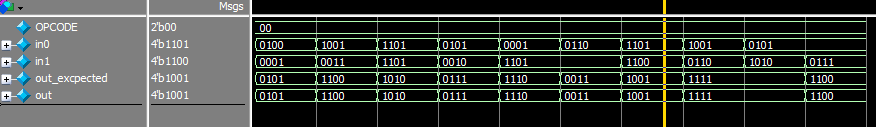
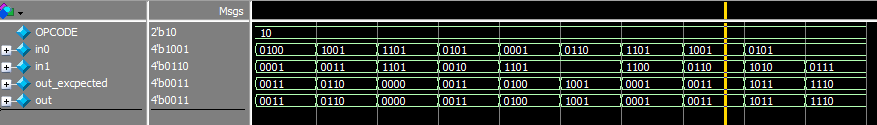
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Figure 4: Q1 Wave (Subtraction)

Figure 3: Q1 Wave (OR)

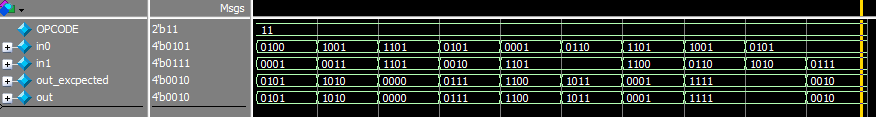
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Figure 5: Q1 Wave (XOR)

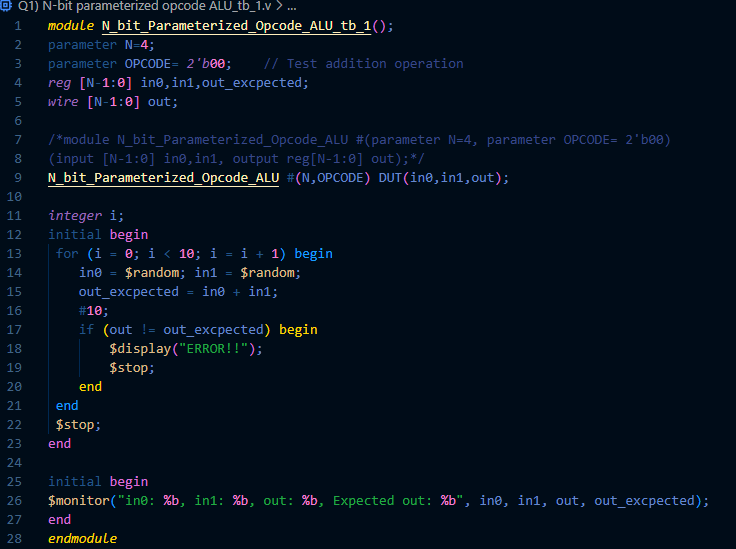
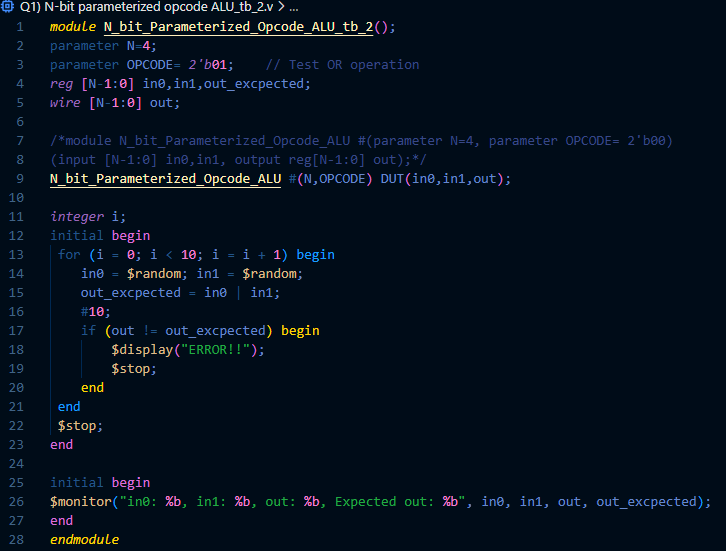
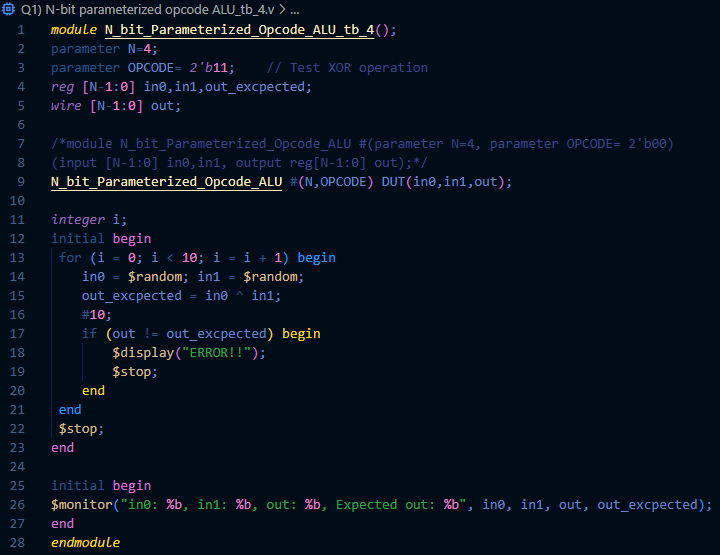
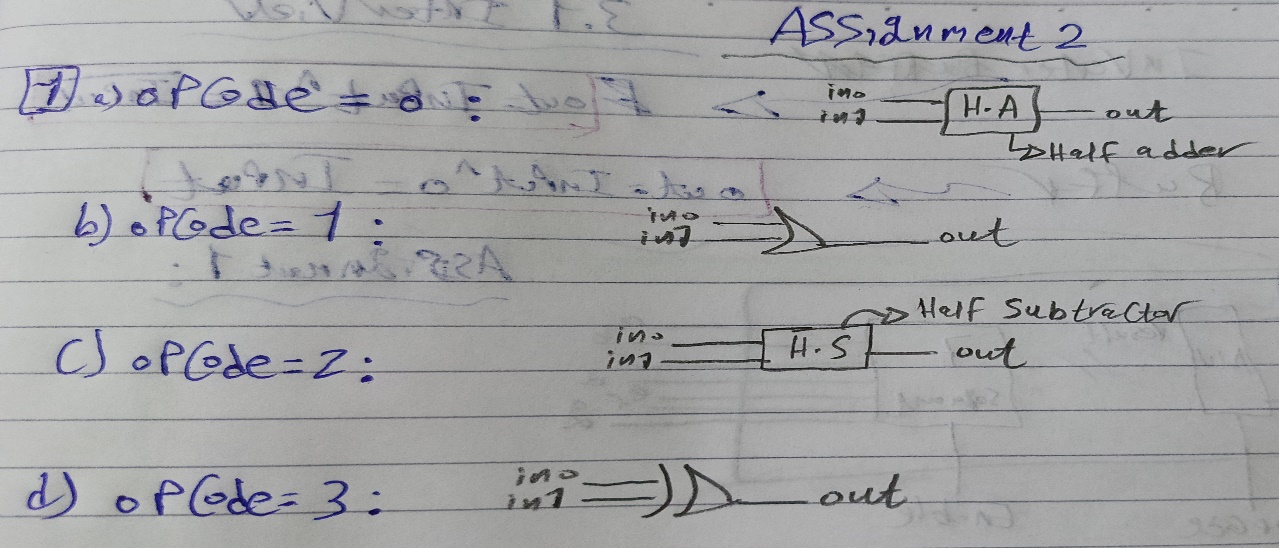
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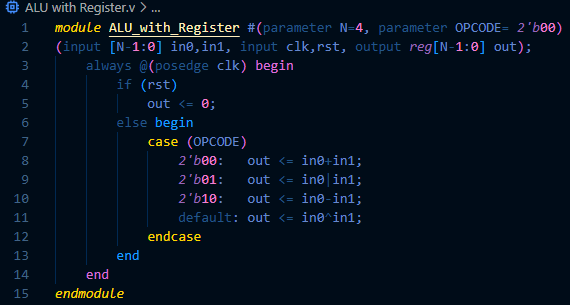
Figure 10: Q1 Synthesis

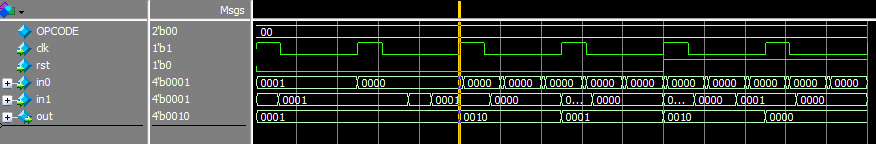
Figure 8: Q1 testbench (Subtraction)

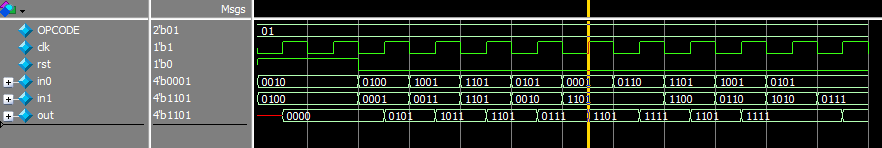
Figure 9: Q1 testbench (XOR)

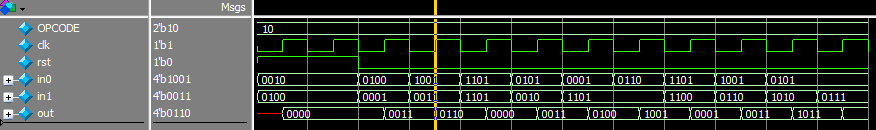
Figure 7: Q1 testbench (OR)

Figure 6: Q1 testbench (Addition)

1. **ALU with Register:**

**** Figure 11: Q2 Code

**** Figure 12: Q2 Wave (Addition)

**** Figure 13: Q2 Wave (OR)

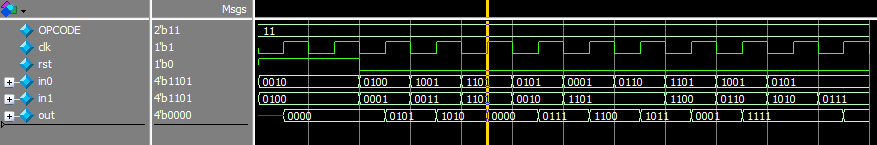
**** Figure 14: Q2 Wave (Subtraction)

Figure 15: Q2 Wave (XOR)

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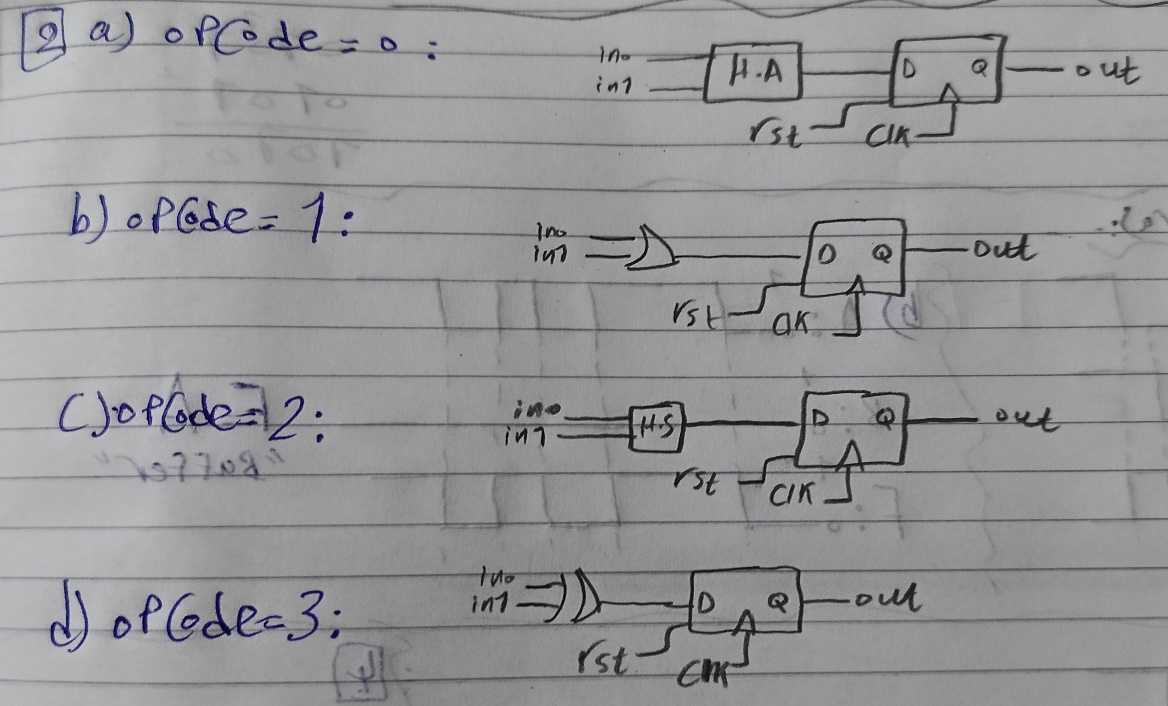
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Figure 16: Q2 Testbench

Figure 17: Q2 Synthesis

1. **Data Latch with active low Clear:**

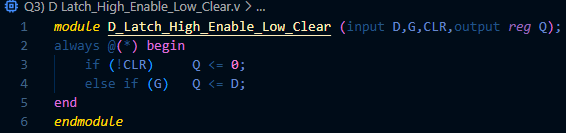
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Figure 18: Q3 Code

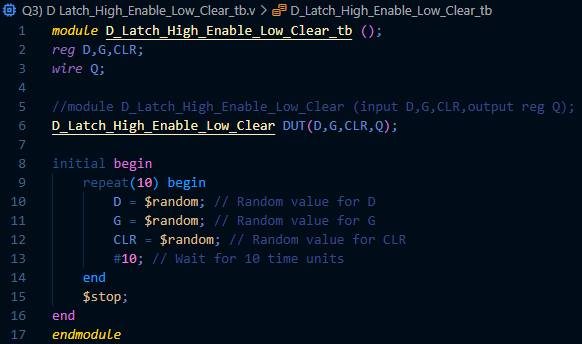
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Figure 19: Q3 Testbench

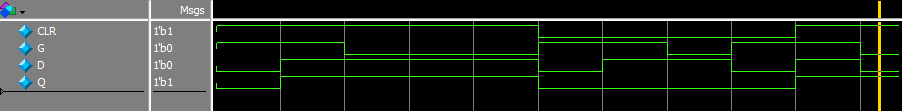
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Figure 20: Q3 Wave

1. **D Latch with Asynchronous set and clr:**

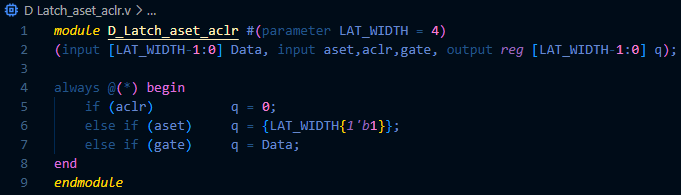
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Figure 21: Q4 Code

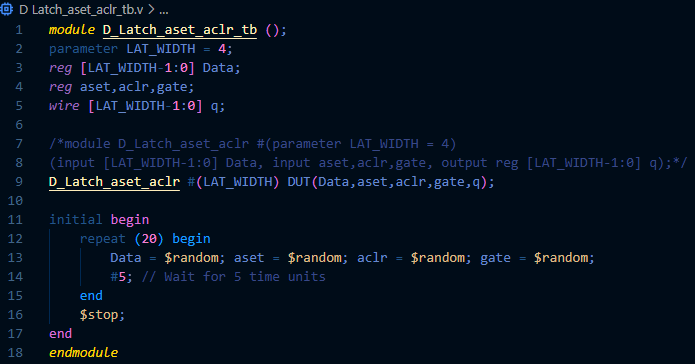
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Figure 22: Q4 Testbench

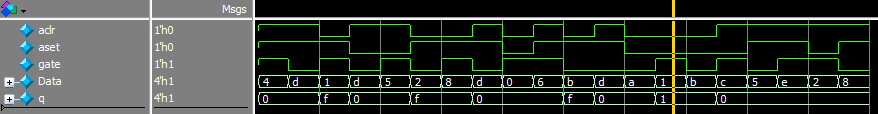
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Figure 23: Q4 Wave

1. **T FF with Asynchronous Active Low rst:**

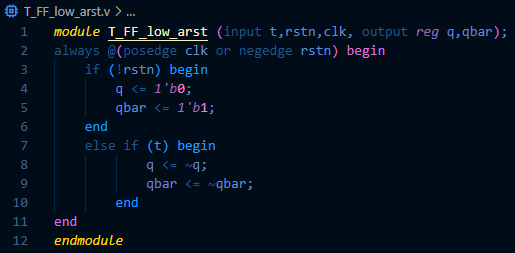
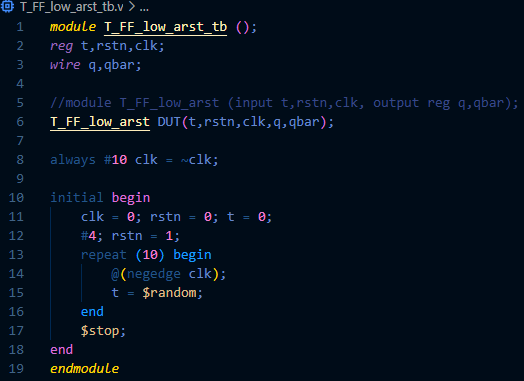
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Figure 24: Q5a Code

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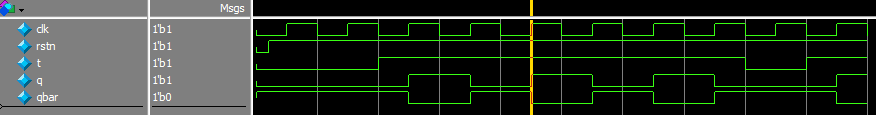
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Figure 26: Q5a Wave

Figure 25: Q5a Testbench

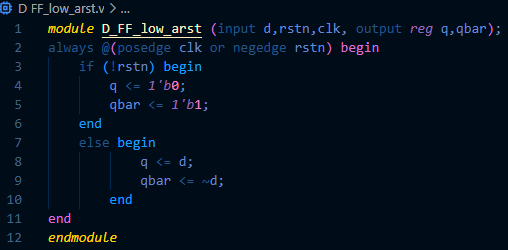
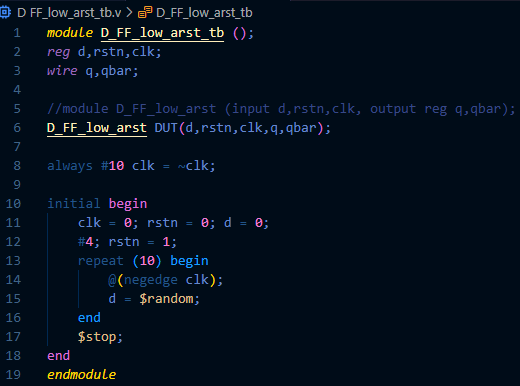
1. **D FF\_low\_arst:**

Figure 27: Q5b Code

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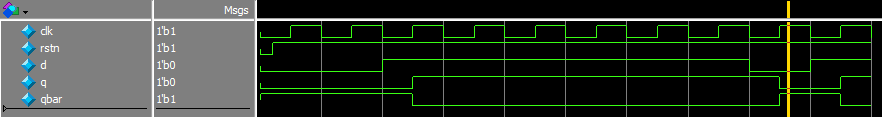
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Figure 29: Q5b Wave

Figure 28: Q5b Testbench

1. **Parameterized Asynchronous FF with Active low rst**

**(D FF & T FF):**

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Figure 30: Q5c Code

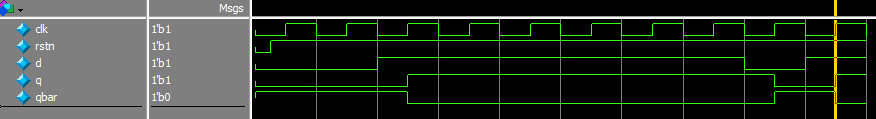
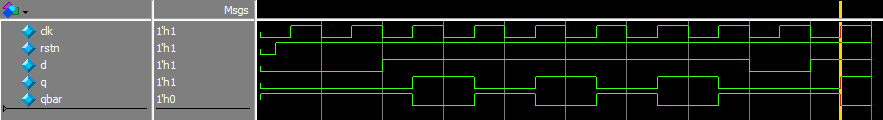
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Figure 32: Q5c Wave (TFF)

Figure 31: Q5c Wave (DFF)

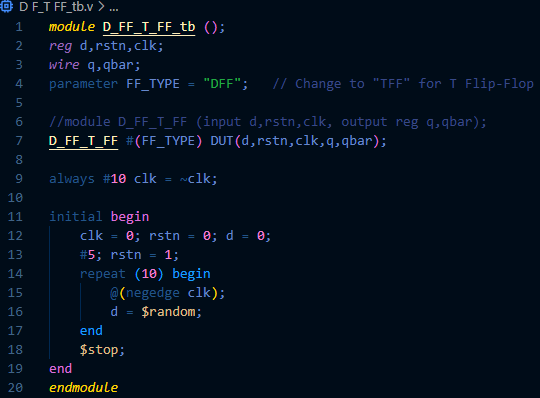
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Figure 33: Q5c Testbench